IN THE SPECIFICATION:

Replace the paragraph bridging pages 12 and 13, specifically page 12, line 24 through page 13, line 5, with the following paragraph:

Although this mode of the invention shows the case where the 3-bit digital picture signal is inputted without division, the digital picture signal to be inputted may be divided to a lower operation frequency of the shift register. In this case, ~~signal transmission lines~~ signals for 3 bits x division number in total are [[put]] input, and shift registers, the number of which is equal to ~~that, becomes~~ the number of bits, become necessary. Incidentally, the number of DFFs contained in the respective shift registers is decreased correspondingly to the division number. An example of a number of shift registers being a multiple of m (i.e., 3) is shown in FIG. 28.